What is claimed is:

1. A vertical dynamic random access memory (DRAM) cell device fabricated within a trench region in a substrate, the trench having first and second opposing substantially vertical edges, the vertical DRAM cell comprising:
(a) a storage capacitor formed within trench region for storing electrical charge;
(b) a transistor formed within the trench region above the storage capacitor;
(c) a buried strap formed proximate to the first vertical edge between the storage capacitor and the transistor, the buried strap electrically coupling the storage capacitor and the transistor; and
(d) an isolation collar region formed proximate to the second vertical edge of the trench, the isolation collar extending the length of the transistor.

2. The cell device according to claim 1, further comprising a trench top oxide (TTO) region comprising a bottom surface, the bottom surface located above a top surface of the buried strap, wherein the trench top oxide and the buried strap are located between the transistor and the storage capacitor.

3. The cell device according to claim 2, wherein the top portion of the buried strap is vertically separated from the bottom surface of the trench top oxide by about 150 to 450 nm.

4. The cell device according to claim 3, wherein the isolation collar has a bottom edge, the bottom edge extending below the vertical location of the buried strap top surface by about 50-1000.

5. The cell device according to claim 3, wherein the isolation collar has a bottom edge, the bottom edge vertically separated from the top surface of the buried strap by about 50-100 nm.

6. The cell device according to claim 4, wherein the buried strap comprises a one-sided strap.

7. The cell device according to claim 6, wherein the one-sided strap has a vertical dimension in the range of about 30 to 150 nm, and a lateral dimension in the range of about 50-100 nm.

8. The cell device according to claim 5, wherein the buried strap comprises a one-sided strap.

9. The cell device according to claim 8, wherein the one-sided strap has a vertical dimension in the range of about 30 to 150 nm, and a lateral dimension in the range of about 50 to 100 nm.

10. A buried strap for electrically connecting a transistor and a storage capacitor in a vertical dynamic random access memory (DRAM) cell device formed within a semiconductor substrate and having a trench with first and second opposing vertical edges, the buried strap comprising: an electrically conducting region formed within the trench, the electrically conducting region formed proximate to the first opposing edge between the transistor and storage capacitor, and laterally displaced from an isolation region formed on the second opposing vertical edge, the isolation region extending from the semiconductor substrate surface along the second opposing vertical edge and terminating at an edge no lower than the electrically conducting region, the buried strap formed at or below edge of the isolation region.

11. The buried strap according to claim 10, wherein the electrically conducting region formed proximate to the first opposing edge is laterally separated from the second opposing edge by about 50-110 nm.

12. The buried strap according to claim 10, wherein the isolation region comprises a shallow trench isolation (STI) region.

13. The buried strap according to claim 10, wherein the shallow trench isolation has a depth no greater than about 250-350 nm.

14. The buried strap according to claim 10, wherein the shallow trench isolation region has a depth no greater than about 50 to 150 nm.

15. The buried strap according to claim 12, wherein the shallow trench isolation region comprises an oxide collar for electrically isolating the transistor and the storage capacitor in the vertical DRAM cell device from potential cross talk with an adjacent DRAM cell device.

16. The buried strap according to claim 10, wherein the electrically conducting region comprises undoped polysilicon.

17. The buried strap according to claim 10, wherein the electrically conducting region comprises doped polysilicon.

18. A method for providing shallow trench isolation in a vertical dynamic random access memory (DRAM) cell device having a storage capacitor and a transistor formed in a trench region, the trench region having a first edge, a

second edge, and a trench bottom, the trench extending vertically downwards from a semiconductor substrate surface to the trench bottom, the method comprising:

(a) isolating a region adjacent to the first edge of the trench, the isolated region extending vertically downwards from the semiconductor substrate surface in the direction of the trench bottom to a preselected depth, wherein the region is isolated from an adjacent DRAM cell device; and

(b) connecting the storage capacitor to the transistor at a connection location adjacent to the second edge of the trench, the connection location laterally displaced from the isolated region adjacent to the first edge, the connection positioned such that the isolated region terminates no lower than the connection location adjacent to the second edge.

19. The method according to claim 18, wherein the region electrically isolates the first edge of the trench from electrical cross-talk.

20. The method according to claim 19, wherein the isolated lateral displacement isolates the connection location from electrical cross talk from the at least one adjacent DRAM cell device which is adjacent to the first edge

21. The method according to claim 18, wherein the lateral displacement of the connection location is selected in order that the region adjacent to the first edge below the depth of the connection location need not be isolated from another cell proximate to the first edge.

22. A method of fabricating an isolation region for shallow trench isolation in a vertical dynamic random access memory (DRAM) cell device having a transistor and a capacitor formed in a trench, the trench having a first edge and an opposing second edge, the method comprising:

(a) lining the first edge and opposing second edge of the trench with an oxide material;

(b) partially filling the trench with polysilicon, the polysilicon having a top surface;

(c) removing the oxide material lining from the first edge of the trench;

(d) forming a divot in the surface of the polysilicon proximate to the first edge of the trench; and

(e) filling the divot in the polysilicon with an electrically conductive material, the electrically conductive material forming a buried strap.

23. The method according to claim 22, further comprising the step of: (f) forming a trench top oxide (TTO) layer over the buried strap and polysilicon.

24. The method according to claim 23, wherein the trench top oxide (TTO) layer isolates the capacitor from signals applied to a gate region of the transistor.

25. The method according to claim 22, wherein the opposing second edge isolates the DRAM cell device from at least one adjacent DRAM cell device.

26. The method according to claim 25, wherein the buried strap is isolated from electrical cross-talk from the at least one adjacent DRAM cell device.

27. The method according to claim 22, wherein the buried strap electrically connects a transistor to a capacitor, wherein the transistor and the capacitor form part of the DRAM cell device.

28. The method according to claim 22, wherein the buried strap comprises a one-sided buried strap (OSS).

29. The method according to claim 28, wherein the one-sided buried strap is laterally displaced from the second opposing edge of the trench, wherein the lateral displacement of the one-sided buried strap substantially provides electrical cross-talk immunity from the at least one adjacent DRAM cell device.

30. The method according to claim 22, wherein the electrically conductive material comprises doped polysilicon.

31. A vertical dynamic random access memory (DRAM) device comprising: a plurality of cell devices, each of the plurality of cell devices comprising a trench having a trench depth and substantially vertical opposing edges, the respective vertical opposing edges of an adjacent pair of the plurality of cell devices separated by a separation width, the ratio between the trench depth and the separation width comprising a value of less than about 1.5.

32. The device according to claim 31, wherein the value of the ratio between the trench depth and the separation width is less than about 1.0